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10EC56

Fifth Semester B.E. Degree Examination, June/July 2014
Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Write a note on evolution of IC era. **(04 Marks)**

b. Explain the basic DC equations used in different regions of operation of MOS device. Identify these regions on V-I characteristics. **(07 Marks)**

c. Explain with necessary circuit diagram and expressions, the body effect and how it affects the threshold voltage. **(04 Marks)**

d. Find the value of body effect parameter (γ) and the threshold voltage V_{th}, when the applied substrate bias is 3V. Given $V_{tho} = 0.4$ V, $N_A = 10^{16}/cm^3$, thermal equivalent voltage = 26mV, $n_i = 1.5 \times 10^{10}/cm^3$, $t_{ox} = 40$ nm, $\epsilon_0 = 8.85 \times 10^{-14}$ F/cm, $\epsilon_{r(si)} = 11.9$, $\epsilon_{r(ox)} = 3.9$, $q = 1.6 \times 10^{-19}$ C. **(05 Marks)**

2 a. Draw the circuit diagram of a 2 i/p CMOS NAND gate along with stick diagram. Explain also the working of the circuit. **(08 Marks)**

b. Explain how layout optimization can be used for increase in speed with an AND gate circuit and stick diagrams. **(12 Marks)**

3 a. Discuss the working, merits and demerits of the following logic structures with two i/p NAND gate realization as an example:
i) Pseudo NMOS logic ii) Complementary CMOS logic. **(10 Marks)**

b. Explain CMOS domino logic with the basic gate and derive the evaluation voltage equation. What are the advantages of this logic? **(10 Marks)**

4 a. What is sheet resistance? Explain the steps involved in calculating the sheet resistance of: i) transistor channel, ii) nMOS inverter, iii) CMOS inverter. **(09 Marks)**

b. A particular layer of MOS circuit has a resistivity of 10 ohm-cm. A section of this layer is 55 μm long and 5 μm wide and has a thickness of 1 μm. Calculate the resistance from one end of this section to the other end. What is the value of Rs.? **(05 Marks)**

c. What is the drawback of conventional inverter? How it is overcome using super buffers? Explain the working of inverting and non-inverting super buffers with necessary diagrams. **(06 Marks)**

PART – B

5 a. Explain the working of switch logic, pass transistor and transmission gates with their merits and demerits. **(08 Marks)**

b. Explain the structural design concept using bus arbitration logic as an example. **(12 Marks)**

6 a. What are the general considerations to be followed in designing a sub system? **(08 Marks)**

b. What are the basic requirements of a shifter? Explain with an example of 4 × 4 crossbar switch. What are the drawbacks of this basic switch and how it is overcome? **(12 Marks)**

7 a. Explain the working of three transistor dynamics RAM cell with circuit and stick diagrams. **(10 Marks)**

b. Mention and explain various VLSI design tools used. Also explain different levels at simulation of VLSI design. **(10 Marks)**

8 Write short notes on: a. I/O pads b. Real estate in VLSI
c. Silicides d. Clocked circuits. **(20 Marks)**

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